REMARKS/ARGUMENTS

Reconsideration of the application in view of the above amendments and the followings remarks is respectfully requested. Claims 1-3 have been cancelled without prejudice. Claims 4-21 have been added.

The Examiner is concerned with the filing of an Information Disclosure Statement and specifically asks whether the representative is aware of other relevant prior art. The undersigned has contacted the inventor and can confirm that as of the present time, neither the inventor nor the undersigned attorney is aware of closer prior art which would be material to the examination of this application.

The Examiner states that Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. A proposed drawing correction is enclosed herewith.

The Examiner rejects claims 1-3 under 35 U.S.C. 102(b) as being clearly anticipated by Bianco et al. The Examiner states that Bianco et al already discloses a method for sensitive circuit protection with set-scan testing.

The Examiner rejects 1-3 under 35 U.S.C. § 102(e) as being clearly anticipated by Ragavachari. The Examiner states that Ragavachari discloses a method for enhancing security in and discouraging theft of VSLI and USLI devices.

We cannot agree that either of these references anticipates the present invention or renders it obvious. In the present invention a plurality of commands are applied to a plurality of input ports for the processor. These commands are then processed by a program stored in the memory of the computer system and is used to generate a password which is compared against the password which has been stored in the system. In one embodiment, of the invention the password command is applied to the processor ports in a prescribed time sequence. This is very different from the systems shown in either of the references recited by the Examiner.

In the references, use is made of a password which is applied to a single input of the system. The systems utilize protection schemes such as a long password thus requiring many iterations to crack the password and then permitting only a small number of attempts at obtaining the password before access to the internal workings of the integrated circuit chip are blocked. This type of scheme works well where access is being attempted against a single computer system. It does not work well where the integrated circuit computer system is mass marketed and thus many integrated circuits are available

for testing. In a mass market product, one attempting to crack the password can simply move from one circuit where the limit at finding the password has been reached to the next integrated circuit and continue the process.

The present invention provides a simple way of making this far more difficult by requiring that a plurality of commands be applied to a plurality of input ports. In one embodiment, these commands are applied in a described sequence, which makes this far more difficult for a thief to crack the password and then gain access to the system. This difficulty is provided without the complexity of circuitry required by the two references recited by the Examiner.

Claims 1-3 have been cancelled without prejudice and replaced with new claims 4-21.

Applicants believe the application as amended is in condition for allowance, and such action is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

Please delete the title and substitute therefor --SECURITY SYSTEM FOR INTEGRATED CIRCUIT COMPUTER SYSTEM--.

In the Claims:

Please cancel claims 1-3 without prejudice.

Please add new claims 4-21 as follows:

--4. (new) An integrated circuit computer system comprising:

a processor interconnected with memory and peripheral circuits on said integrated circuit;

a scan-path interface circuit for reading out contents of a predetermined memory or register in said system;

a switching circuit coupled to said processor and to said scan-path interface circuit for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled; and

security means comprising:

a plurality of input ports for said processor;

a program stored in said memory to operate said process to receive a plurality of commands applied to said plurality of input ports and to process said commands to produce a password which is compared with a predetermined password;

and wherein said switching circuit is responsive to said comparison.

5. (new) The computer system of claim 4 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

6. (new) The computer system of claim 4 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

7. (new) The computer system of claim 5 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

8. (new) In an integrated circuit computer system having a processor interconnected with memory and peripheral circuits on said integrated circuit and coupled to a scan-path interface circuit, a security system comprising:

a plurality of input ports for said processor;

a program stored in said memory to operate said processor to received a plurality of commands applied to said plurality of input ports and to process said commands to produce a password which is compared with a predetermined password.

9. (new) The security system of claim 8 further comprising a switching circuit coupled to said scan-path interface circuit and responsive to said comparison for switching said scan-path interface circuit between a first mode in which it is enabled and a second mode in which it is disabled.

10. (new) The security system of claim 8 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

11. (new) The security system of claim 8 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

12. (new) The security system of claim 9 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

13. (new) The security system of claim 10 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers for controlling said switching circuit.

14. (new) A security system for an integrated circuit computer system comprising:

means for applying a plurality of commands to a plurality of ports for a processor of said system;

a program stored in a memory coupled to said processor for operating said processor to process said plurality of commands to produce a password;

means for comparing said produced password with a predetermined password.

15. (new) The security system of claim 14 wherein said program operates said processor to receive said plurality of commands which are applied to said plurality of ports in a specific time sequence.

16. (new) The security system of claim 14 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

17. (new) The security system of claim 15 further comprising a pair of registers, one of said registers receiving said produced password and the other of said registers containing said predetermined password; and a comparator for comparing the contents of said registers and generating a comparison signal.

18. (new) The security system of claim 14 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and disabled modes.

19. (new) The security system of claim 15 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

20. (new) The security system of claim 16 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.

21. (new) The security system of claim 17 further comprising a scan-path interface circuit for reading out contents of a predetermined memory or register in said system and a switching circuit responsive to said comparison to switch operation of said scan-path interface circuit between enabled and a disable modes.--

In the Drawings:

A proposed drawing correction is enclosed herewith.